Digital Offboard Interface to the Fermilab Internet Rack Monitor

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July 16, 1993

This note describes the external digital interface board used in the Fermilab Internet Rack Monitor. This board is interfaced by a 50-pin ribbon cable to an IndustryPack™† driver mounted on the MVME-162 computer. External connections to this board are designed to be the same as the earlier Smart Rack Monitor, and similar to the DZero Rack Monitor.

The Internet Rack Monitor's extrernal digital interface is implemented by a the board shown in Figure 1. This board provides 8 bytes of general purpose digital I/O and the connection to a front panel LED display.

The eight bytes of digital I/O are available through four 37S "D" connectors that are configured to match the digital I/O of previous rack monitors. The pinout of these connectors are shown in Figyre 2. In addition to the 16 binary bits, a separate strobe is available to indicate an access to each byte of data, and one pin indicates the data direction of the transfer. Plus 5V is also available to operate small external devices such as temperature sensors. The data direction of each byte is fixed by an 8-bit DIP switch. The configuration of this switch can be read by the computer.

In addition to the eight bytes of digital I/O, two 8-bit latches are included for operating front pannel LED indicators. These LEDs supplement the byte of LEDs and the byte of switches input that are interfaced to the IP driver module on the MVME-162 cpu card.

Two small relays on the board are intended for use as contacts in an external interlock chain. Typically, these relays would be operated by the software if some fault or abnormal operating condition was found in the equipment controlled by the Internet Rack Monitor. This board also provides for a connection of the event clock and an additional trigger to the digital interface IP module.

All the logic nessary for address decoding, write strobe and read enable generation is handled by the Actel 1010 FPGA. These gate arrays are now a cost effective way to implement logic function normally done by PALs. The pinout for the Actel part is given in Figure 3.

All connections between this card and the MVME-162 are made by the 50-pin ribbon cable connector shown in Figure 4 along with the front panel connector pinout. A slight modification of the gate array will allow a second digital I/O board to be connected to the same ribbon cable if more digital I/O is needed.

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† IndustryPack and IP are trademarks of GreenSpring Computers, Inc.

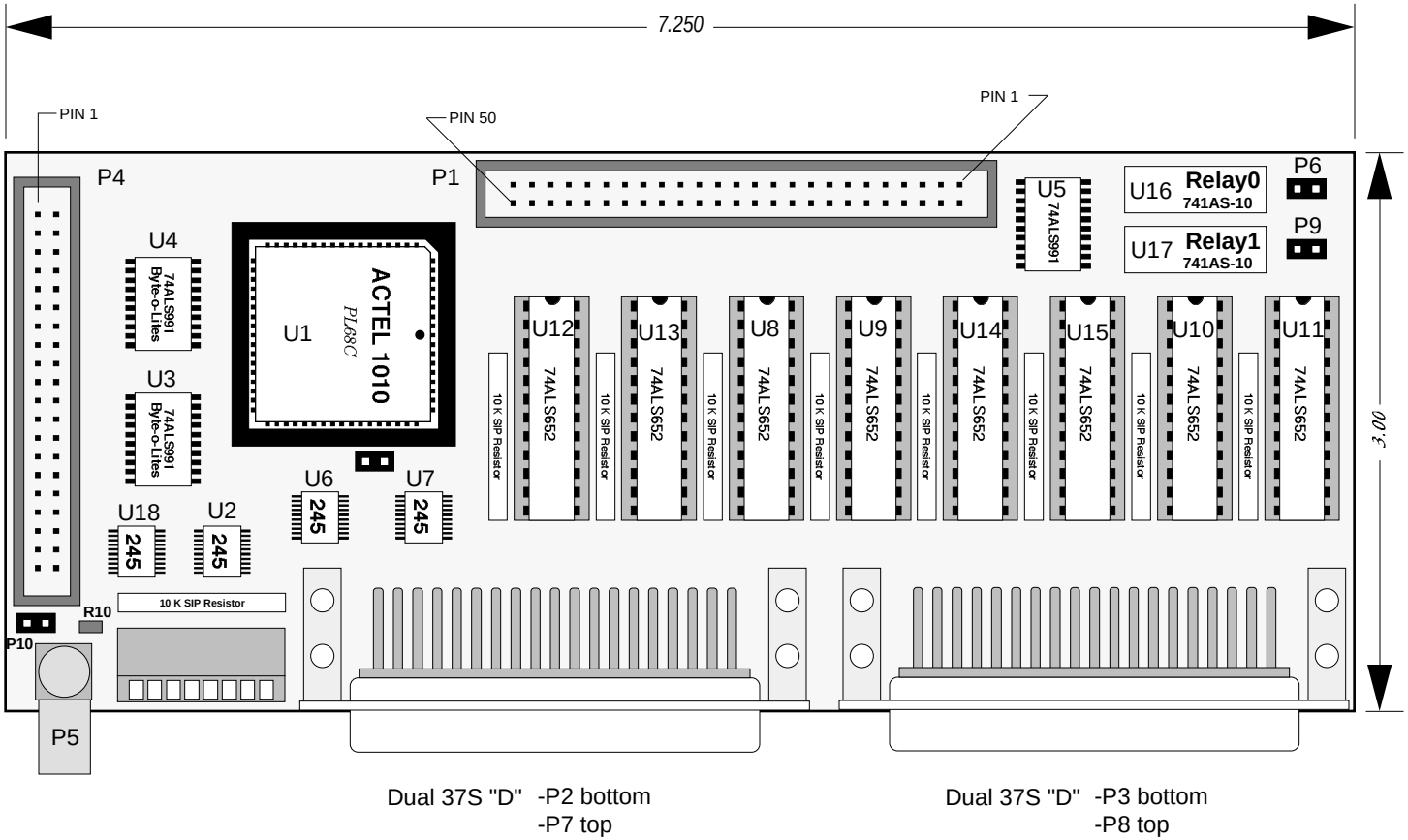


Figure 1. FIRM Digital Offboard

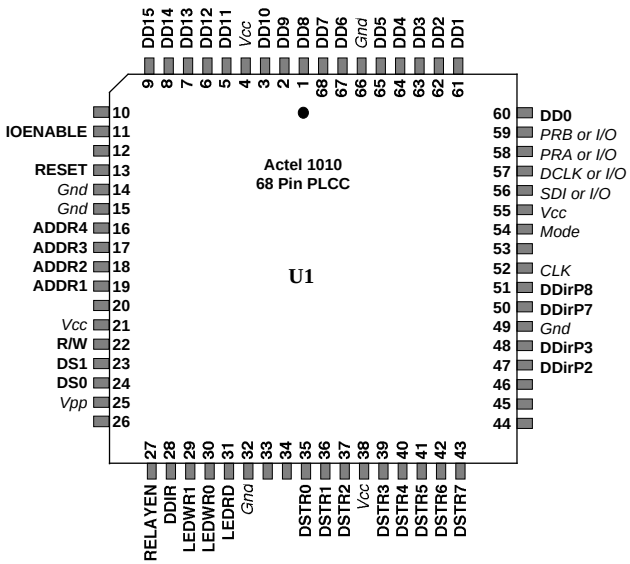
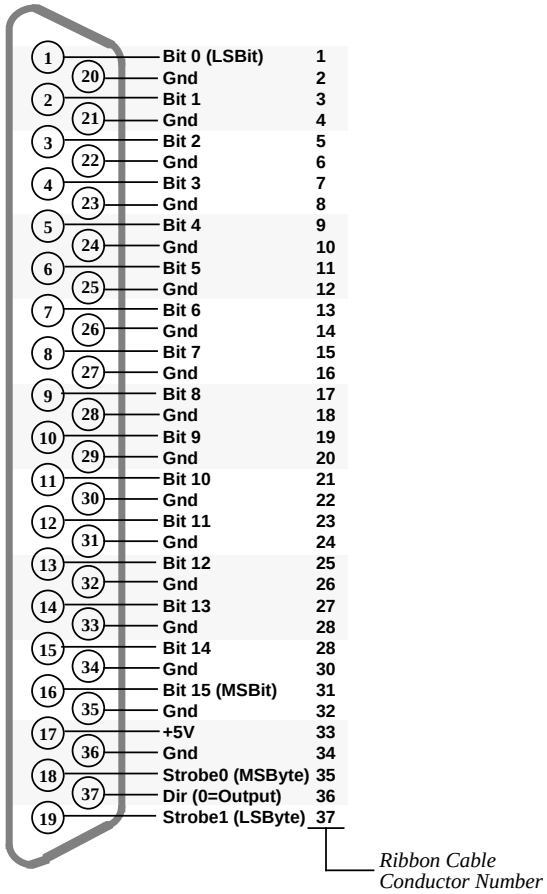
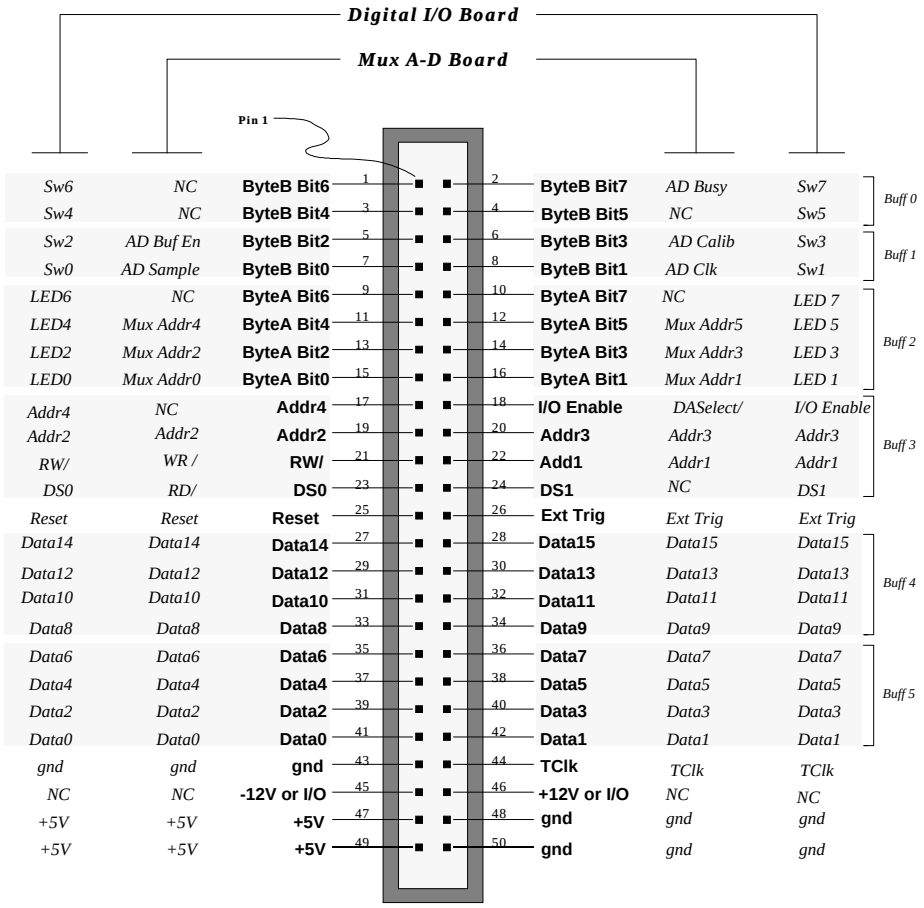


Figure 2. FIRM Digital Offboard FPGA

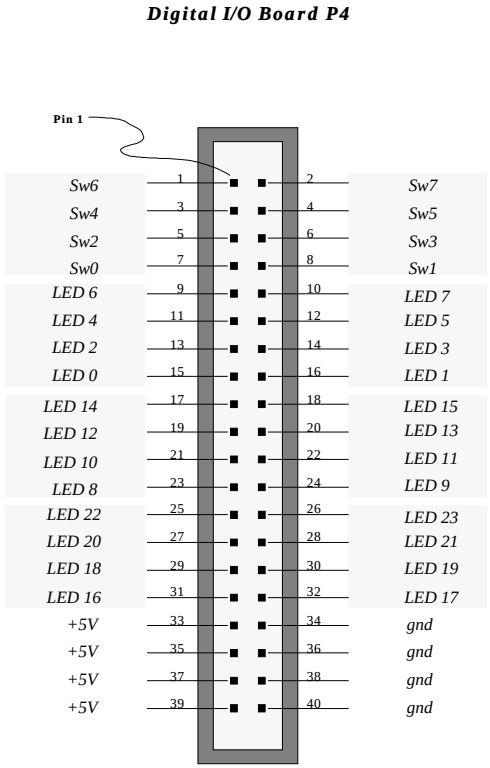


Note: Strobes are short positive pulses. Output data is valid on the trailing (high to low) transition of the strobe pulse.

Figure 3. FIRM Digital Output Connectors P2, P3, P7, and P8



a. I/O Interface Connector P1



b. Front Panel Interface Connector P4

Figure 4. Connector pinouts

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